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Amendments to the Specification:

Please replace paragraph [0022] with the following amended paragraph:

[0022] To overcome this problem the second current source **30** and respective switch **39** are provided. A second digital input code **32** is fed to the second current source **30** via second input line **29**. The second digital input code comprises single bit data and is derived from the first digital input code. Preferably, the second current source **30** is disposed adjacent to the first current source 3. Preferably, the second current source **30** is identical to said first current source 3, preferably including the output load. With respect to the output load, it is commented that in a system, components, such as a cable [[t]]line, an antenna, etc. will be connected to the output nodes **23, 36**. Further, downstream of the output nodes **23, 36**, a further component will register the output signal. These components put a load on the digital to analog converter, and are referred to as the "output load". Sometimes the output load is heavy, which means that it absorbs a lot of power. If this is the case, the converter will need to supply a lot of power on a single output line, if the output signal, in the present invention, the output current is high, and less if the output signal is low. The effect of this is that the digital to analog converter will experience a signal dependent "kick back", which depends on the output load. It will be understood that while the above description of the output load influence is essentially a static one, it may become even more of a problem dynamically, that is when a current source switches. It has been found that the response of the switching on the global lines[[,]] is also partly a result of the response due to the output load. So, preferably, if the response of the shadow switching on the global lines is to be equal to that of the switching of the first current sources, the output loads of both output lines are preferably matched. Thus, preferably, the output loads associated with first and second nodes **23, 36, 26, 37** are substantially matched.